Claims

[c1] 1. A semiconductor IC structure comprising:
a semiconductor substrate including at least one front-end-of-the-line device (FEOL) located on a surface thereof;
at least one resistor located on, or in close proximity to, said surface of said semiconductor substrate, said at least one resistor comprising at least a conductive metal; and
first level of metallization above said at least one resistor.

[c2] 2. The semiconductor IC structure of Claim 1 further comprising a trench isolation region in said semiconductor substrate, said at least one resistor is positioned on said trench isolation region.

[c3] 3. The semiconductor IC structure of Claim 1 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

[c4] 4. The semiconductor IC structure of Claim 3 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

[c5] 5. The semiconductor IC structure of Claim 1 wherein said conductive metal has a thickness from about 20 to about 50 nm.

[c6] 6. The semiconductor IC structure of Claim 1 further comprising an etch stop layer located beneath said conductive metal.

[c7] 7. The semiconductor IC structure of Claim 6 wherein said etch stop layer has a thickness from about 20 to about 50 nm.

[c8] 8. The semiconductor IC structure of Claim 1 further comprising a dielectric material on said at least one resistor.

[c9] 9. The semiconductor IC structure of Claim 1 wherein said first level of

metallization comprises an interlevel dielectric material having contact openings that are filled with a conductive material.

[c10] 10. The semiconductor IC structure of Claim 1 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

[c11] 11. A method for integrating a metal resistor into a CMOS technology comprising the steps of:
forming at least one FEOL device on a surface of a semiconductor substrate;
forming at least one resistor on, or in close proximity to, the surface of said semiconductor substrate, said at least one resistor comprising a conductive metal; and
forming a first level of metallization over said semiconductor structure.

[c12] 12. The method of Claim 11 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

[c13] 13. The method of Claim 11 wherein said semiconductor substrate includes a trench isolation region and said at least one resistor is formed thereon.

[c14] 14. The method of Claim 11 wherein said forming said at least one resistor comprises forming an etch stop layer over said at least one FEOL device; forming a conductive metal on said etch stop layer; forming a dielectric material on said conductive metal; and patterning said conductive metal and said dielectric material to provide a stack including said conductive metal and said dielectric material.

[c15] 15. The method of Claim 11 wherein said forming said at least one resistor comprises providing a planarized dielectric material on said surface of said semiconductor substrate including said at least one FEOL device; forming a conductive metal on said planarized dielectric material; forming a dielectric material on said conductive metal; and patterning said conductive metal and said dielectric material to provide a stack.

[c16] 16. The method of Claim 11 wherein said forming said at least one resistor comprises forming a silicide metal layer over said semiconductor substrate including said at least one FEOL device; forming a dielectric material over said silicide metal layer; patterning said dielectric material and said silicide metal layer to provide at least one stack on said surface of said semiconductor substrate; and annealing to convert the silicide metal layer of said stack into a metal silicide, wherein said metal silicide of said stack comprises a conductor of a resistor.

[c17] 17. The method of Claim 11 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

[c18] 18. The method of Claim 17 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

[c19] 19. The method of Claim 11 wherein said conductive metal has a thickness from about 20 to about 50 nm.

[c20] 20. The method of Claim 11 wherein said forming said first level of metallization comprises forming an interlevel dielectric material; providing contact openings in said interlevel dielectric; and filling said contact openings with a conductive metal.

[c21] 21. A method for integrating a metal resistor into a CMOS technology

comprising the steps of:

providing a structure including at least one FEOL device located on a surface of a semiconductor substrate;

forming an etch stop layer over said structure including said at least one FEOL device;

forming a conductive metal on said etch stop layer;

forming a dielectric material on said conductive metal;

patterning said conductive metal and said dielectric material to provide a stack including said conductive metal and said dielectric material; and

forming a first level of metallization over said at least one FEOL device and said stack.

[c22] 22. The method of Claim 21 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

[c23] 23. The method of Claim 21 wherein said semiconductor substrate includes a trench isolation region and said at least one resistor is formed thereon.

[c24] 24. The method of Claim 21 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, or SiCr.

[c25] 25. The method of Claim 24 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

[c26] 26. The method of Claim 21 wherein said conductive metal has a thickness from about 20 to about 50 nm.

[c27] 27. The method of Claim 21 wherein said etch stop layer has a thickness from about 20 to about 50 nm.

[c28] 28. A method for integrating a metal resistor into a CMOS technology comprising the steps of:

providing a structure including a planarized dielectric material located on a surface of a semiconductor substrate that comprises at least one FEOL device located thereon;

forming a conductive metal on said planarized dielectric material;

forming a dielectric material on said conductive metal;

patterning said conductive metal and said dielectric material to provide a stack; and

forming a first level of metallization over at least said stack, said planarized dielectric and said at least one FEOL device.

[c29] 29. The method of Claim 28 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

[c30] 30. The method of Claim 28 wherein said semiconductor substrate includes a trench isolation region and said at least one resistor is formed thereon.

[c31] 31. The method of Claim 28 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, or SiCr.

[c32] 32. The method of Claim 31 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

[c33] 33. The method of Claim 28 wherein said conductive metal has a thickness from about 20 to about 50 nm.

[c34] 34. The method of Claim 28 wherein said planarized dielectric material comprising an oxide.

[c35] 35. A method for integrating a metal resistor into a CMOS technology comprising the steps of:

providing a structure including at least one FEOL device located on a surface of a semiconductor substrate;

forming a silicide metal layer over said structure;

forming a dielectric material over said silicide metal layer;

patterning said dielectric material to provide at least one stack of a patterned dielectric material atop a portion of said silicide metal layer, said at least one stack is located atop said surface of said semiconductor substrate;

siliciding to convert at least the silicide metal layer of said stack into a metal silicide, wherein said metal silicide of said stack comprises a conductor of a resistor; and

forming a first level of metallization over at least said stack and said at least one FEOL device.

[c36] 36. The method of Claim 35 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

[c37] 37. The method of Claim 35 wherein said silicide metal layer comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

[c38] 38. The method of Claim 35 wherein said siliciding comprising a first anneal that performed at a temperature from about 300° to about 600°C

[c39] 39. The method of Claim 38 wherein following said first anneal a wet etch process is employed removed to selectively remove unreacted silicide metal layer.

[c40] 40. The method of Claim 39 further comprising a second anneal as part

of said siliciding, said second anneal is performed at a temperature from about 600° to about 800°C.